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	1 Field									
	SF 1		SF 2		SF 3		SF 4		SF 5	
	Address	Sustain = 16	Address	8		4		2		1
Input luminance =16										
Input luminance =15										

Figure 1

	Field										
Sustains per subfield	1	2	5	10	18	28	42	60	83	111	
Number of Combinations											Output luminance
0											
1	1										1
2	1	2									3
3	1	2	5								8
4	1	2	5	10							18
5	1	2	5	10	18						36
6	1	2	5	10	18	28					64
7	1	2	5	10	18	28	42				106
8	1	2	5	10	18	28	42	60			166
9	1	2	5	10	18	28	42	60	83		249
10	1	2	5	10	18	28	42	60	83	111	360

Figure 2

Figure 3

8 Bits Binary
Digital Data

1

Normalization
Circuit

2

Frame Row Column

Gamma
and
Dither Mapping

3

Error Diffusion

4

Random
Numbers

Frame Row Column

Dither

5

4 Bits to
Frame Buffer

6
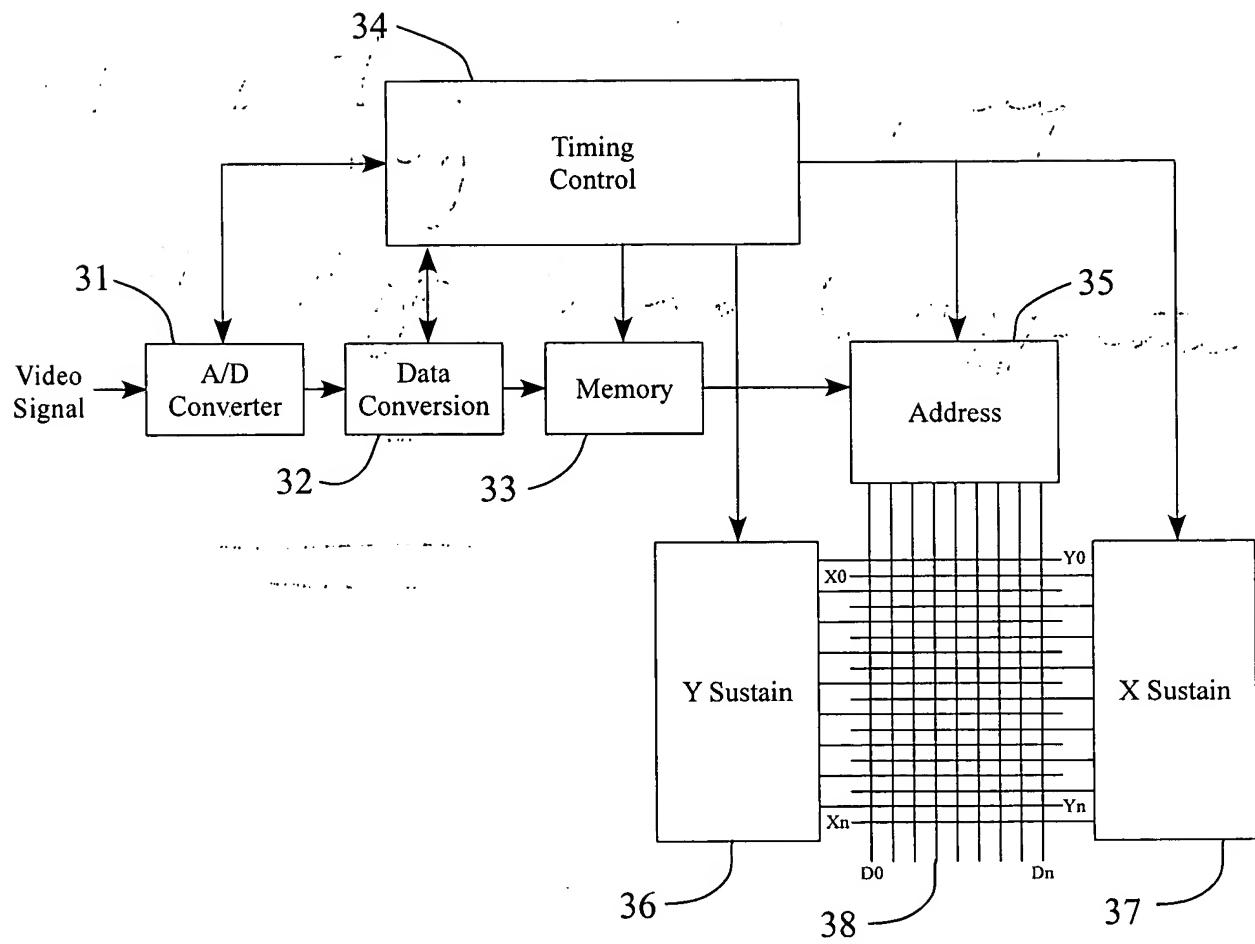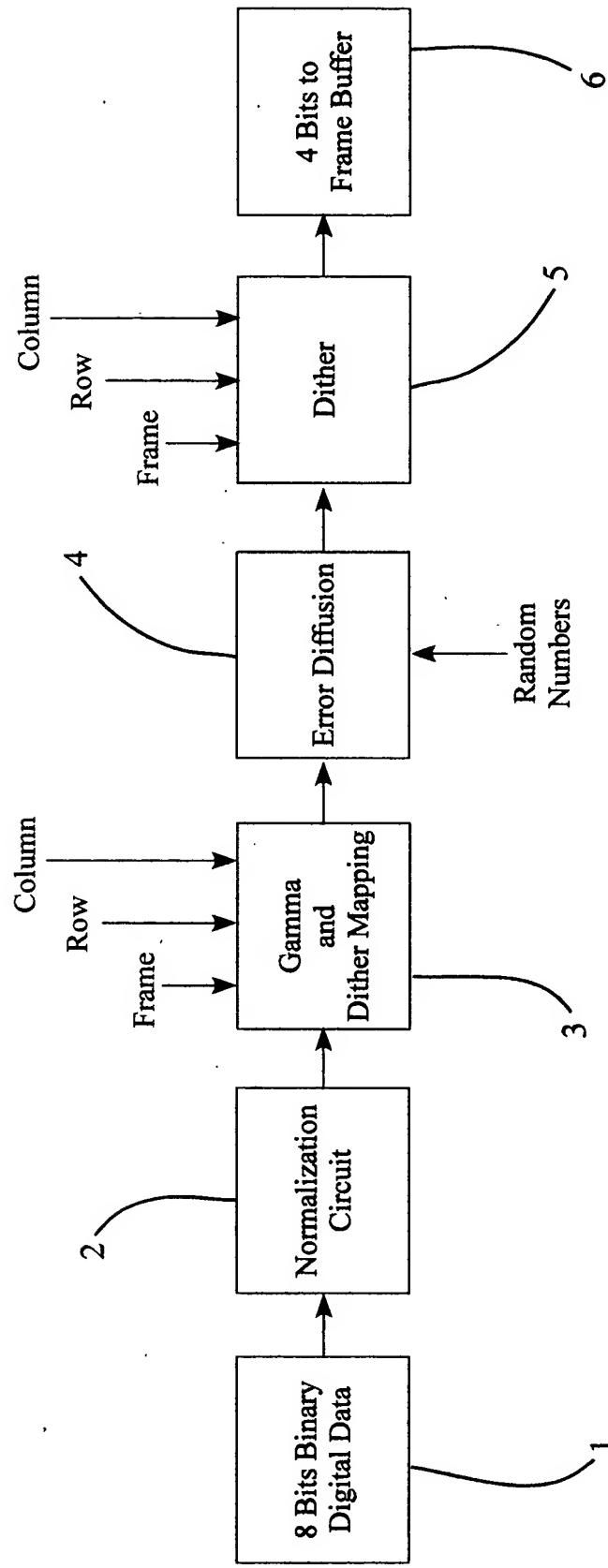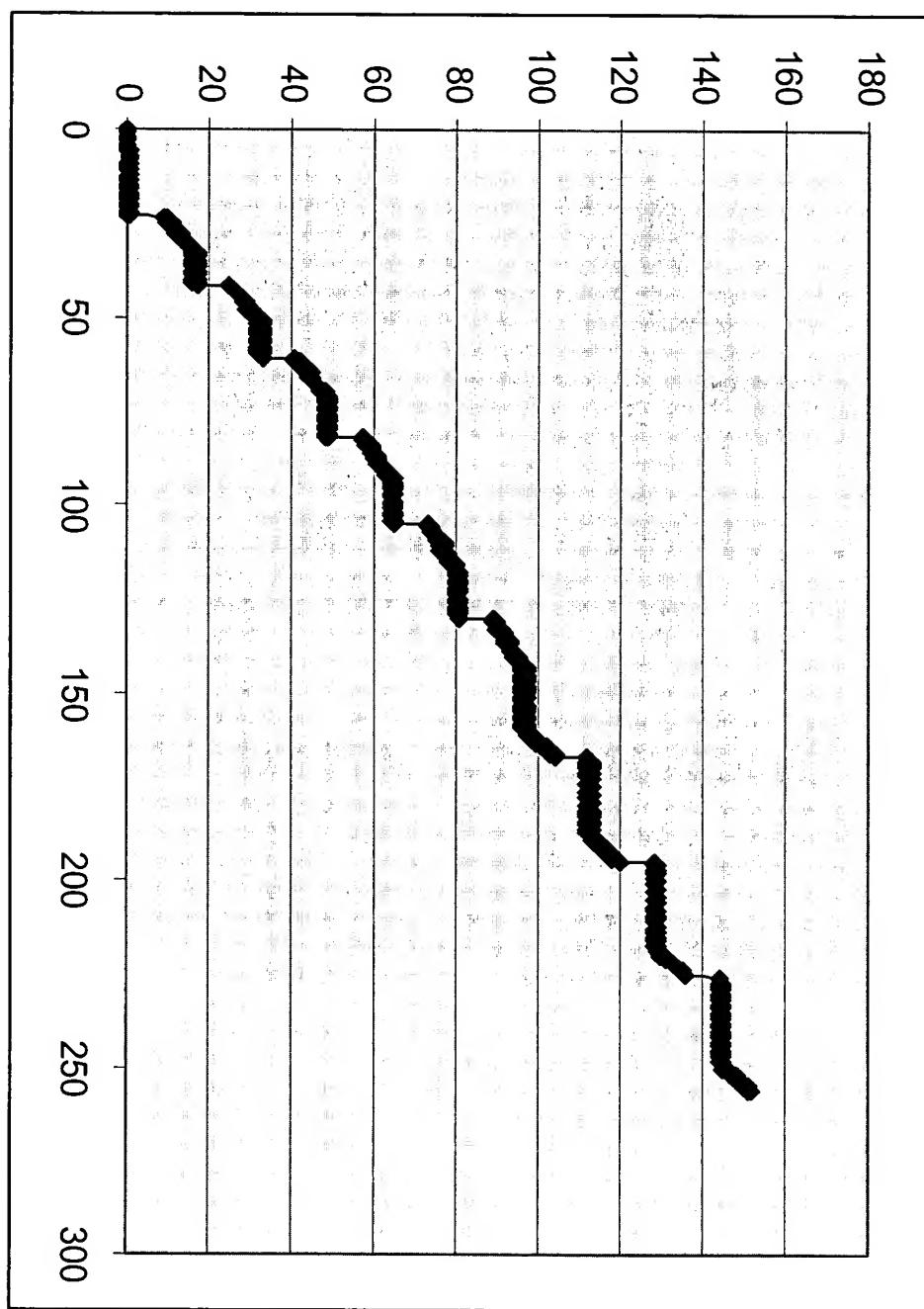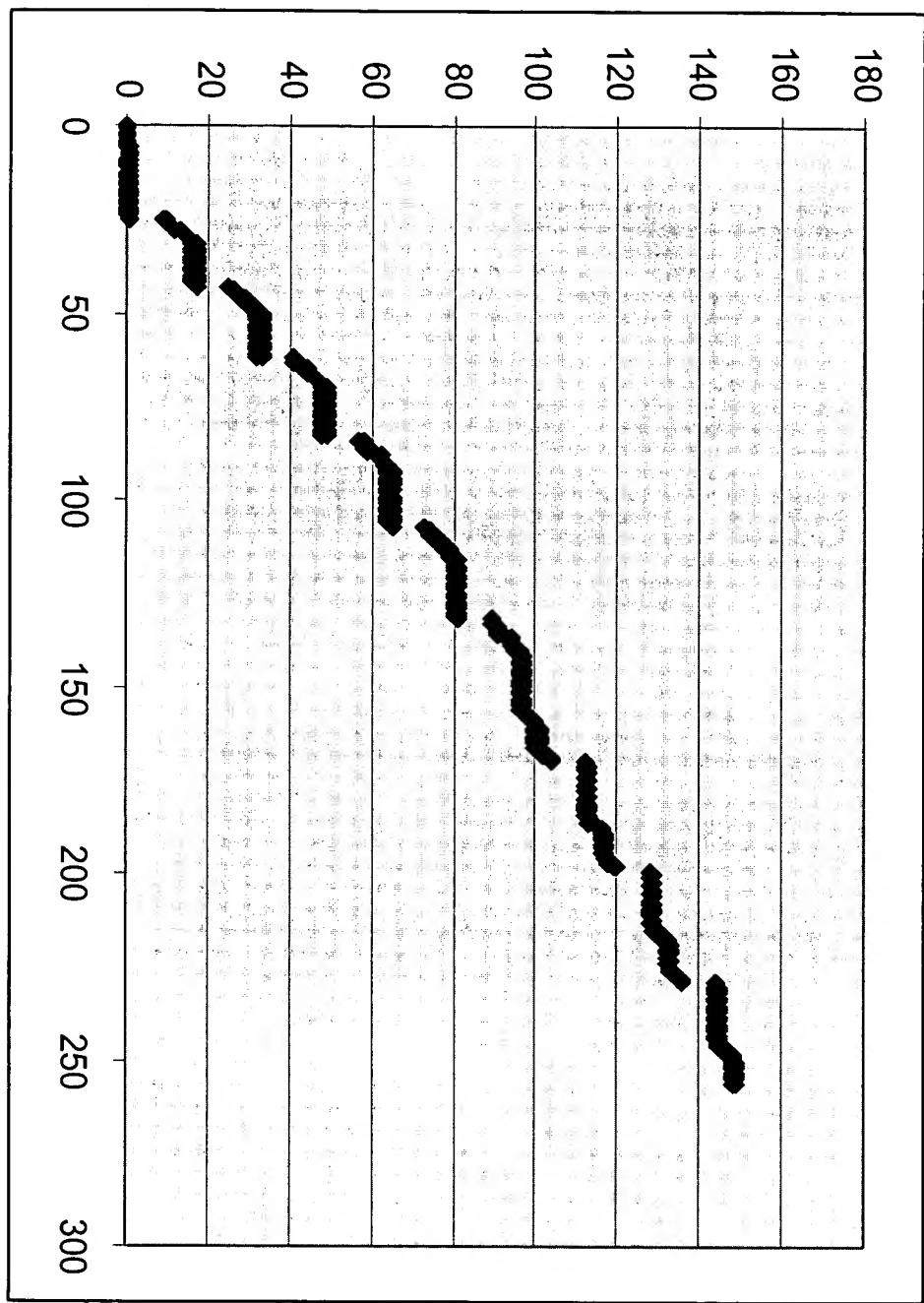
Figure 4

Figure 5a

**Figure 5b**
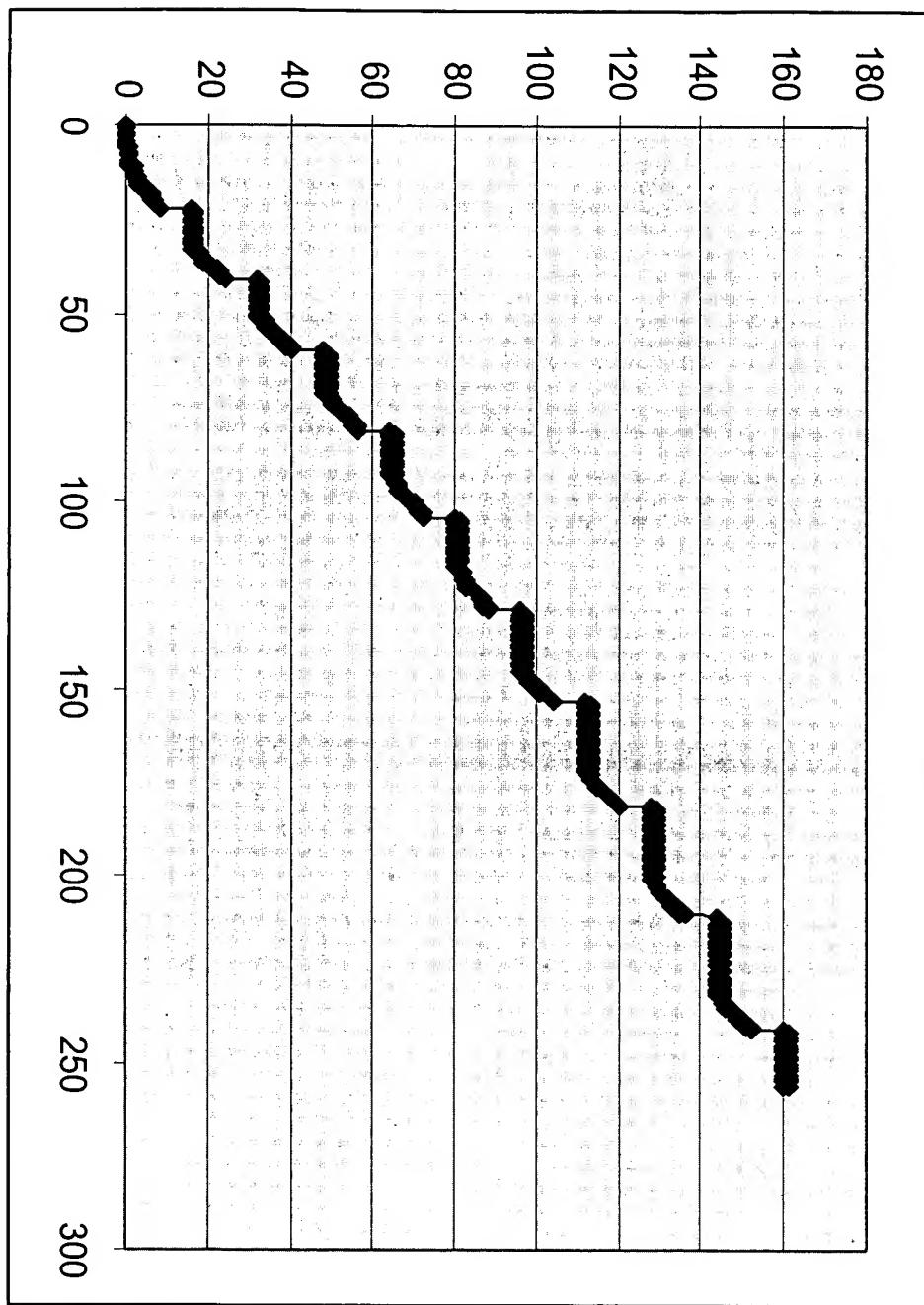
Figure 5c

Figure 5d

Figure 5e

$$E_C = K_{NW}{}^*E_{NW} + K_N{}^*E_N + K_{NE}{}^*E_{NE} + K_W{}^*E_W + K_C{}^*LSB$$

Figure 6

Figure 7

Pixels Upper Left Corner

Odd Remainder   Even Remainder

MRO(1..0)   8   X16 D   9   +D   9   D   9   D   9   +D   4
Clk-4   Clk-3   Clk-2   Clk-1   Clk-0

carry

Odd Remainder

Rand[7..4]   +D
Clk-4

4 (MSB's)   x5D   8
Clk-1

MRE(1..0)   8   X16 D   9   D   9   +D   9   D   9   D   4
Clk-4   Clk-3   Clk-2   Clk-1   Clk-0

carry

Even Remainder

Rand[7..0]   +D   9
Clk-3

Rand[3..0]

Even Remainder

FIFO
1024
x
4   4   x5D   8   +D   8
Clk-5   Clk-4

Odd Remainder

FIFO
1024
x
4   4   x7D   8
Clk-5   Clk-5
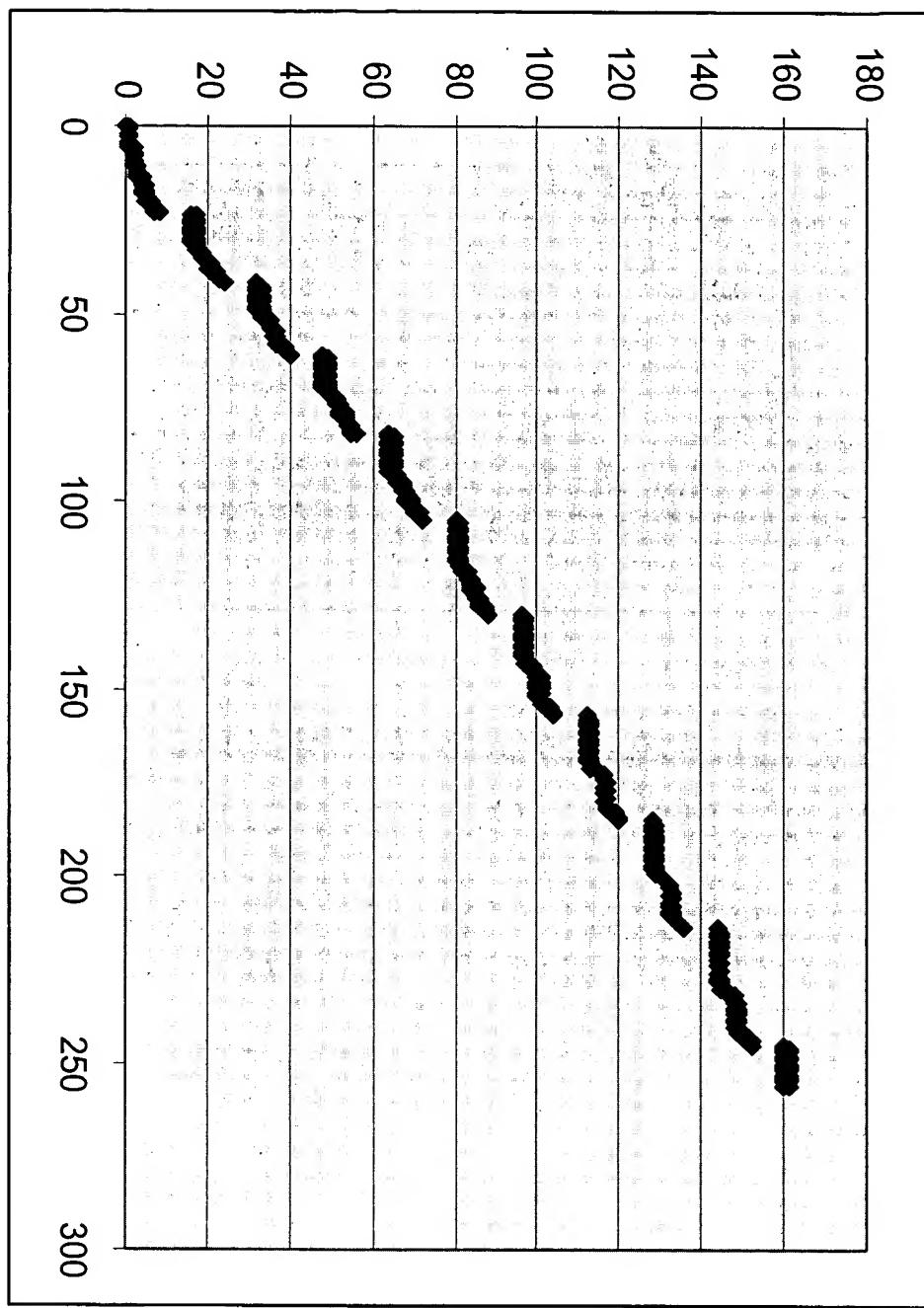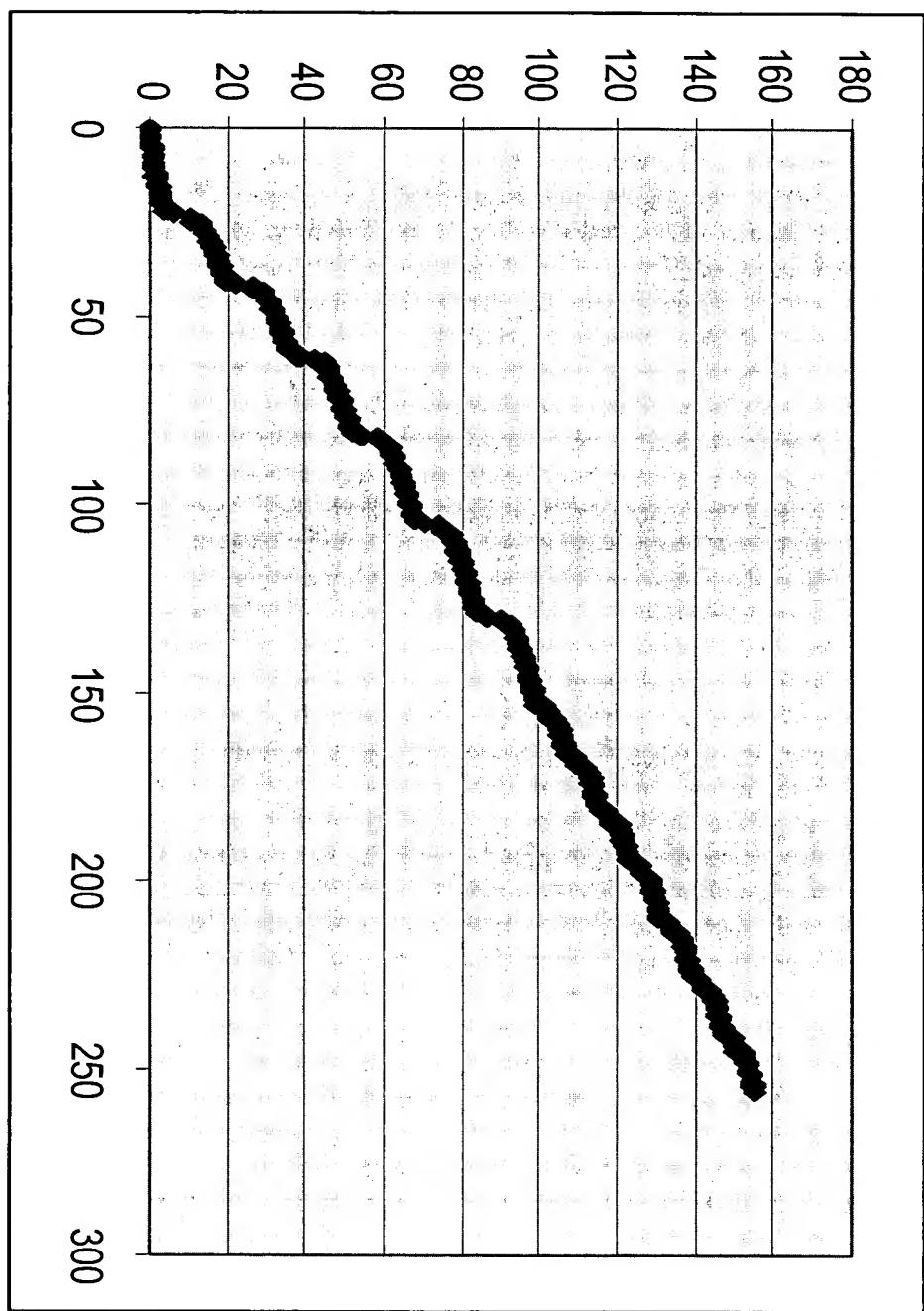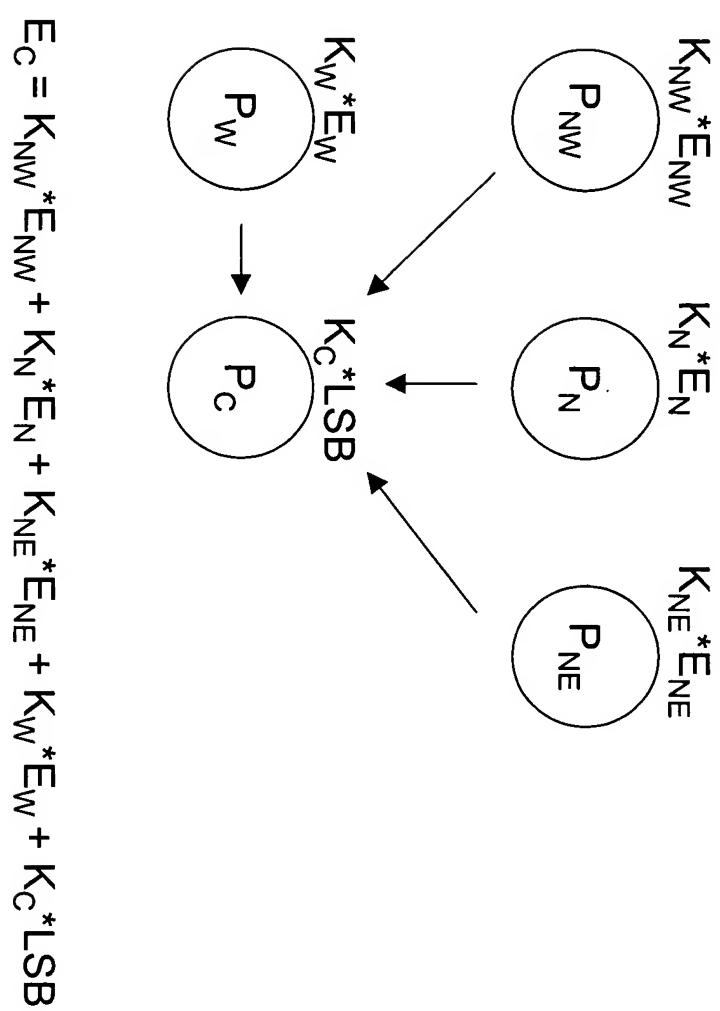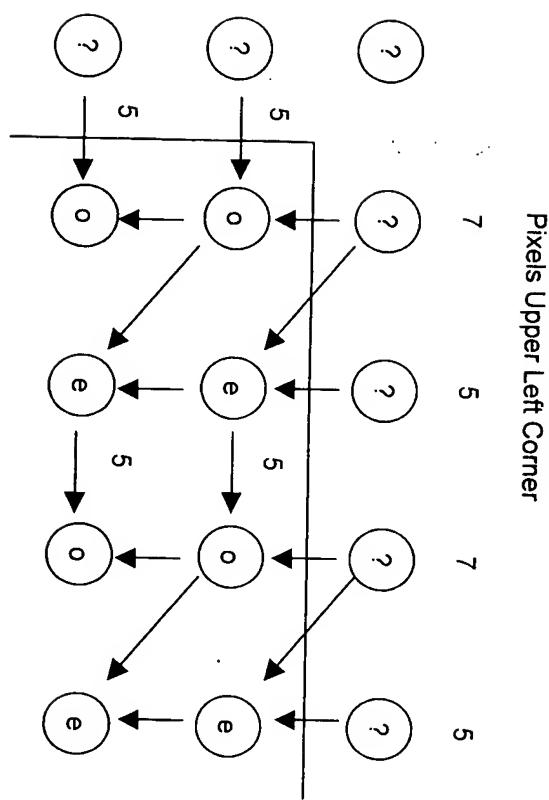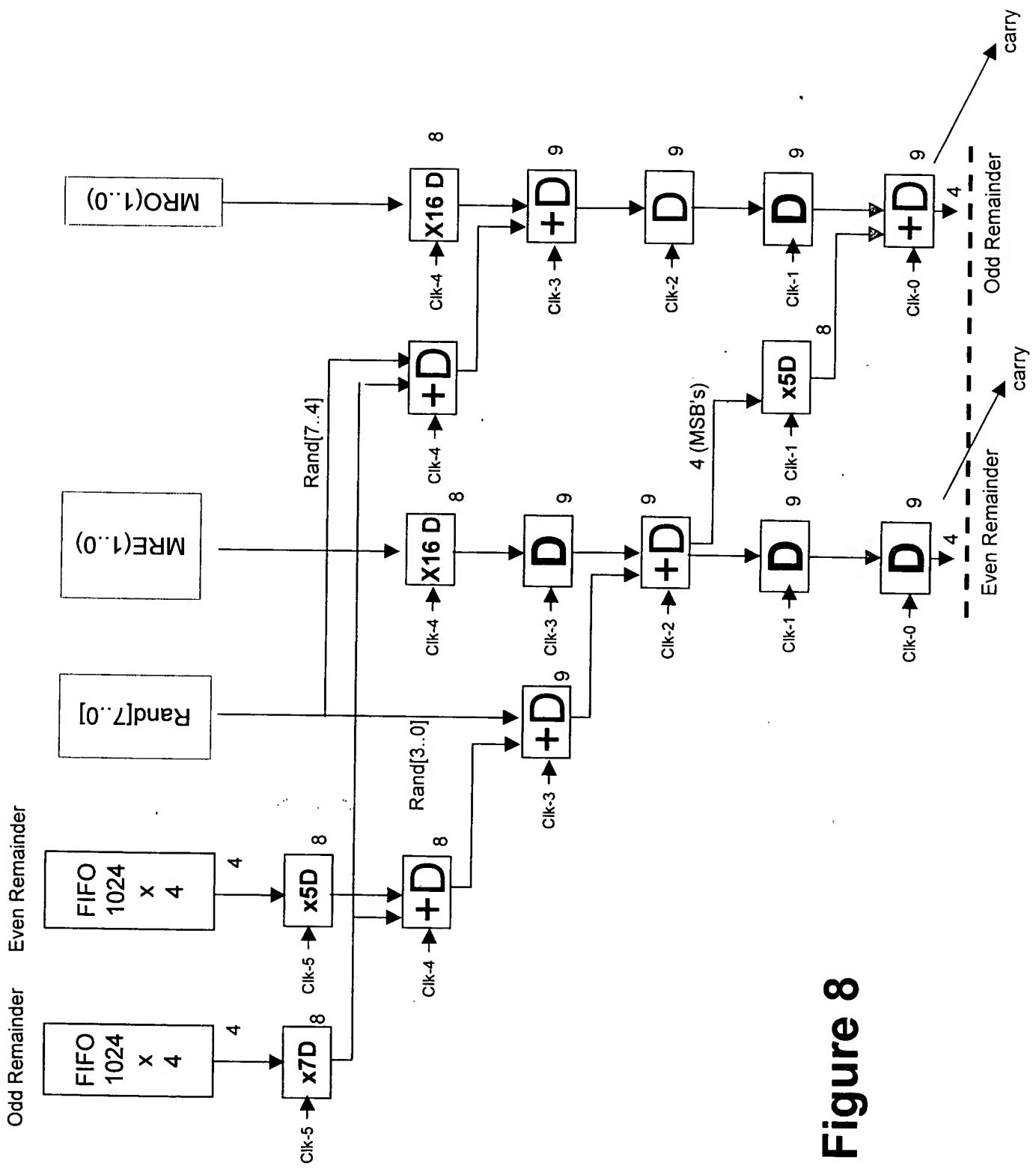
Figure 8

Frame 1

1	2
3	4

Frame 2

2	1
4	3

Frame 3

4	3
2	1

Frame 4

2	1
4	3

Repeat Frame 1

Figure 9a

Pixel Turn-On Order, Low Luminace Input

Frame 0

1	9	3	11
15	7	13	5
3	11	1	9
13	5	15	7

Frame 1

6	14	8	16
12	4	10	2
8	16	6	14
10	2	12	4

Frame 2

3	11	1	9
13	5	15	7
1	9	3	11
15	7	13	5

Frame 3

8	16	6	14
10	2	12	4
6	14	8	16
12	4	10	2

Figure 9b

Pixel Turn-On Order, High Input Luminance

Frame 0

1	14	2	13
16	3	15	4
8	11	7	12
9	6	10	5

Frame 1

7	12	8	11
10	5	9	6
2	13	1	14
15	4	16	3

Frame 2

1	14	2	13
16	3	15	4
8	11	7	12
9	6	10	5

Frame 3

7	12	8	11
10	5	9	6
2	13	1	14
15	4	16	3

Figure 9c

Pixel Turn-On Order, Low Input Luminace

Frame 0

8	3	6	4
1	5	2	7
6	4	8	3
2	7	1	5

Frame 1

5	1	8	4
3	6	2	7
8	4	5	1
2	7	3	6

Frame 2

6	4	8	3
2	7	1	5
8	3	6	4
1	5	2	7

Frame 3

8	4	5	1
2	7	3	6
5	1	8	4
3	6	2	7

Figure 9d

Pixel Turn-On Order, High Input Luminace

Frame 0

2	8	1	7
6	4	5	3
1	7	2	8
5	3	6	4

Frame 1

1	7	2	8
5	3	6	4
2	8	1	7
6	4	5	3

Frame 2

1	7	2	8
5	3	6	4
2	8	1	7
6	4	5	3

Frame 3

2	8	1	7
6	4	5	3
1	7	2	8
5	3	6	4

Figure 9e

Dither Coefficient Lookup

Figure 9f

Both dither tables loaded with same values. Upper 4 bits are even dither value, lower 4 bits are odd dither values.

*sf_table[] = 0 for 10 sf mode, 1 for 12 sf mode
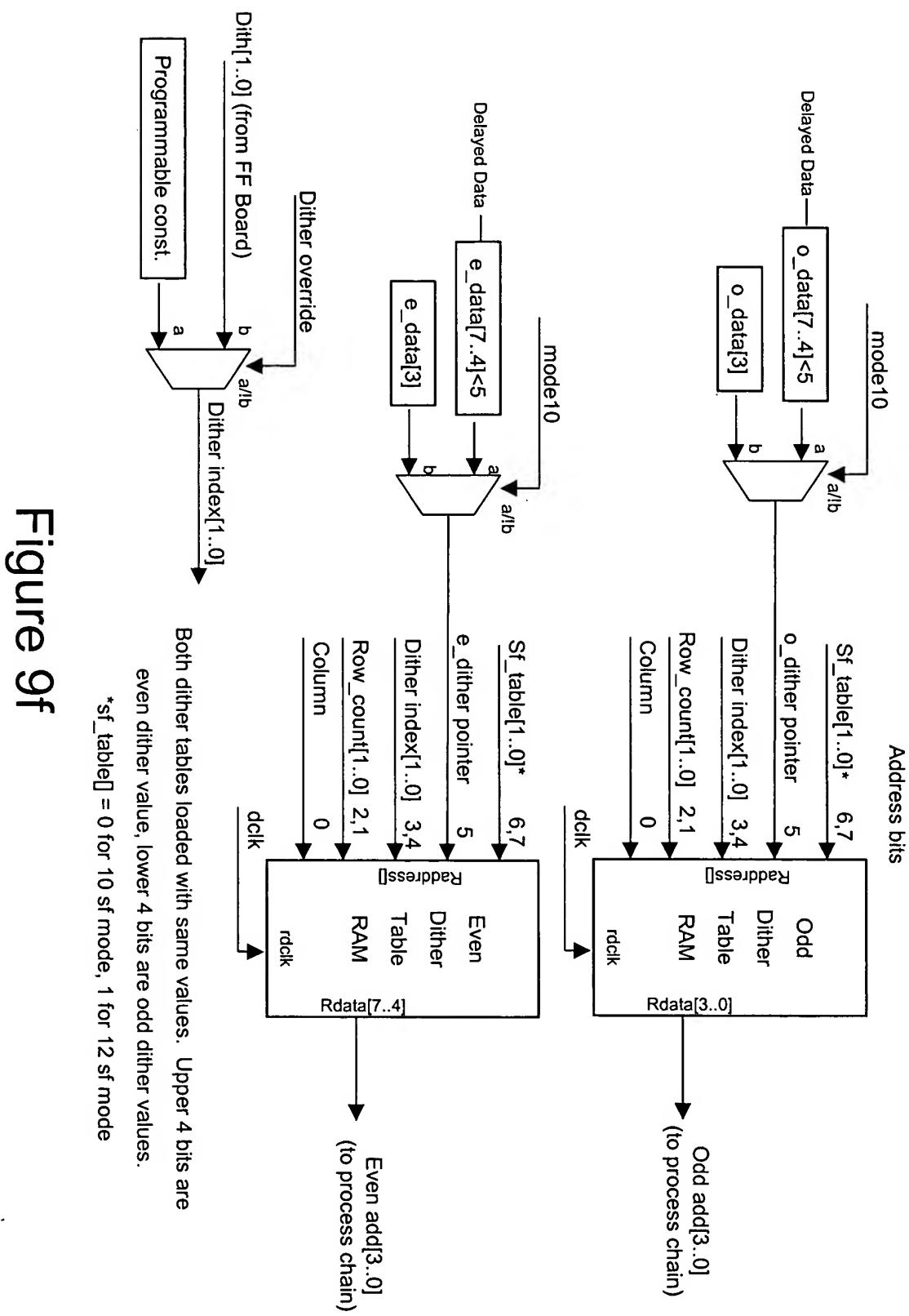
Light Pulse Min and Max APL

Figure 10

CHANNEL 19
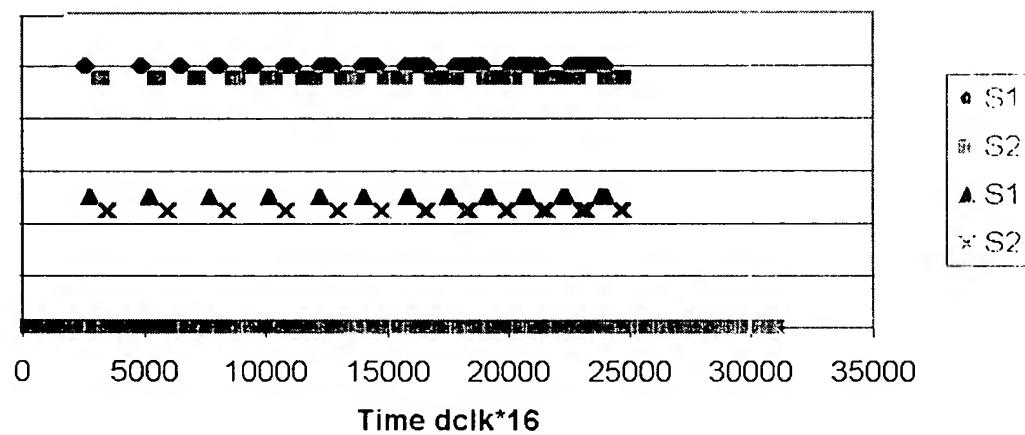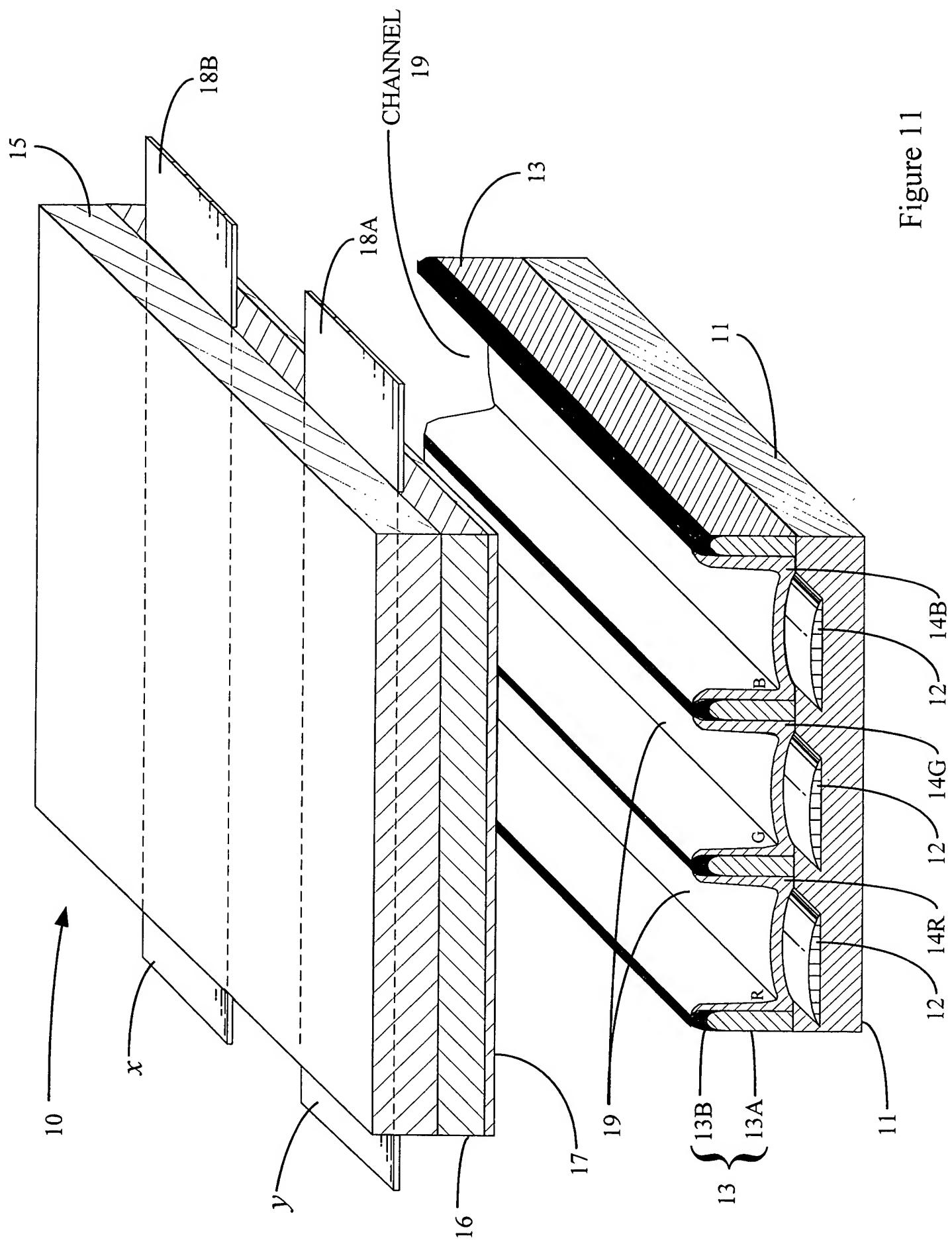
Figure 11
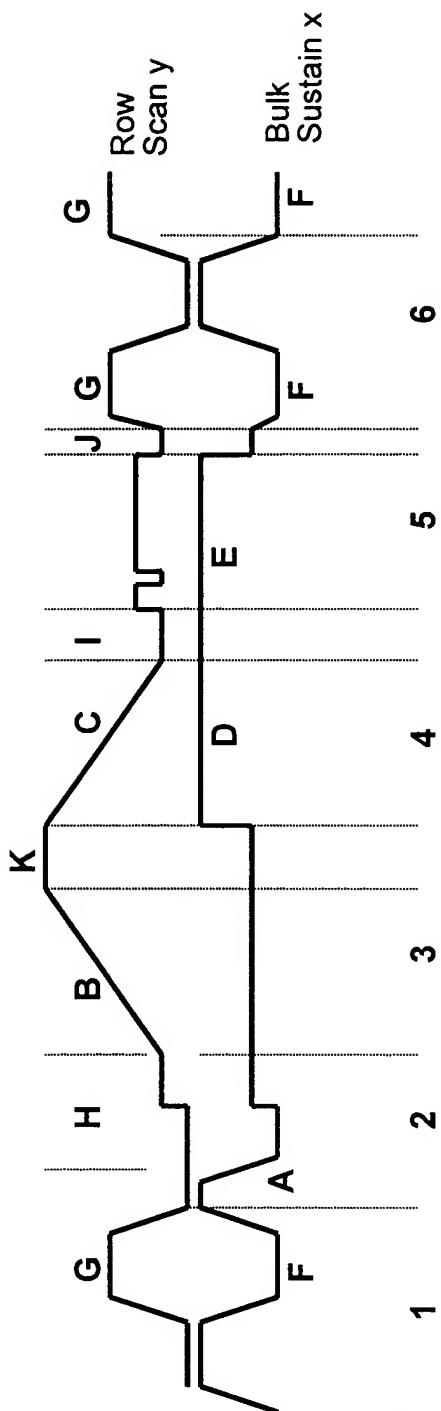
Figure 12

1   SUSTAIN PHASE
2   PRIMING PHASE FOR RAMP RESET
3   UP RAMP RESET
     K- IDLE TIME BEFORE NEGATIVE RAMP RESET
4   DOWN RAMP RESET
     I- IDLE TIME BEFORE ADDRESSING
5   ADDRESSING
   J- IDLE TIME BEFORE SUSTAINING
6   SUSTAIN PHASE

PDP SECTION
S1

PDP SECTION
S2

Figure 13

Figure 14

Figure 15

Row Scan
Electrode
y

Bulk Sustain
Electrode
x

x Sustainer
Section 1
Circuitry — 61A

x Sustainer
Section 2
Circuitry — 61B

x Sustainer
Section 3
Circuitry — 61C

x Sustainer
Section n
Circuitry — 61n

x

x

x

x

50A

50B

50C

50n

PDP 50

CD

Row Scan
Electrode y
Addressing
Circuitry

Row Scan
Electrode y
Addressing
Circuitry

Row Scan
Electrode y
Addressing
Circuitry

Row Scan
Electrode y
Addressing
Circuitry

y

y

y

y

66A

66B

66C

66n

y Sustainer
Section 1
Circuitry

y Sustainer
Section2
Circuitry

y Sustainer
Section 3
Circuitry

y Sustainer
Section n
Circuitry

65A

65B

65C

65n

COLUMN DATA ELECTRONIC CIRCUITRY

57

Column Data Electrode   CD